REMARKS

Present Status of the Application

The Office Action mailed March 26, 2004 rejected all presently pending claims 1-8. Specifically, claims 1-3 and 5-8 were rejected under 35 U.S.C. 102(b) as being anticipated by Cappelletti (US 5,497,345). Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti, in view of some existing knowledge in the art. Reconsideration of claims 1-8 is respectfully requested.

Discussion of Rejections of Claims 1-3 and 5-8 under 35 U.S.C. 102(b)

Claims 1-3 and 5-8 were rejected under 35 U.S.C. 102(b) as being anticipated by Cappelletti, wherein claims 2, 3 and 5-8 are dependent from independent claim 1.

The features of this invention include a polysilicon protection line that electrically connects the word line and a grounded doped region and has a resistance higher than that of the word line. The feature is recited in independent claim 1 as follows, remarked by underlines:

> 1. A non-volatile read only memory device, comprising:
> a word line formed over a substrate, wherein the word line includes a metal layer and a polysilicon line;
> a trapping layer located between the word line and the substrate; and
> a polysilicon protection line formed over the substrate, the protection line electrically connects the word line and a grounded doped region in the substrate, wherein a resistance of the polysilicon protection line is higher than that of the word line.

The Office Action considers that Cappelletti discloses a non-volatile ROM device including a poly-Si protection line 23 & 24 (extending from the word line 7 to the grounded

doped region 29) formed over the substrate 2, which electrically connects the word line 7 and the grounded doped region 29 and has a resistance higher than that of the word line 7 (Fig. 3 and col. 4, line 53-col. 5, line 7).

However, Applicants respectfully point out that Cappelletti actually fails to teach or suggest the above feature of claim 1, since 1) the composite line 23 & 24 is a polycide (poly-Si+silicide) line but not a poly-Si line, 2) the region 29 is a part of the diode D but not a grounded doped region, and 3) col. 4, line 53-col. 5, line 7 and the other parts of Cappelletti's specification do not describe that the composite line 23 & 24 between the word line 7 and the doped region 29 has a higher resistance. The differences are further explained as follows.

(1) As described in col. 4, lines 4-5 of Cappelletti, the composite line 23/24 extending from the word line 7 to the doped region 29 is the combination of a polycrystalline silicon layer 23 and a silicide (WSi_2) layer 24. That is, the composite line 23/24 is a polycide (poly-Si+silicide) line, but not a poly-Si line as in this invention.

(2) As shown in FIG. 3, the doped region 29 is N-doped, the substrate 2 is P-doped, and the doped region 29 and the substrate 2 together constitute a diode "D". However, as recognized in the art, a grounded doped region should have ***the same conductivity type*** as the substrate so that an electric current can readily flow to the substrate through the grounded doped region. Since the conductivity type of the doped region 29 is ***different from that of the substrate 2*** and ***there is a carrier depletion region at the PN junction*** (the

interface between the N-doped region 29 and the P-doped substrate 2), the doped region 29 is not a grounded doped region as recognized in the art.

(3) The Office Action considers that col. 4, line 53-col. 5, line 7 of Cappelletti indicate that the composite line 23/24 between the word line 7 and the diode D has a resistance higher than that of the word line 7. However, Applicants do not find any word discussing the resistance of the composite line 23/24 in the two corresponding paragraphs and the other paragraphs of Cappelletti's specification.

More specifically, the paragraph of col. 4, lines 53-63 discusses about the formation of the second poly-Si layer 23, the doped regions 29 and the corresponding diode D, the silicide layer 24, the gate regions and the S/D regions, etc., as recited below:

"The second polysilicon layer 23 is then deposited and doped in the usual manner, as shown by arrows 34, and the doping species employed also penetrate inside substrate 2 at the active areas 100 of the diodes to produce regions 29 (FIG. 9). At this point, diodes D are complete, and begin operating so as to remove any excess charges from polysilicon layer 23. The rest of the process comprises the usual steps (not shown) of depositing silicide layer 24 (FIG. 3), patterning the gate regions of the circuit transistors and the cells, forming the drain and source regions, and forming the protective layers and connections."

On the other hand, the paragraph from col. 4, line 64-col. 5, line 7 discusses about the working mechanism and the function/effect of the diode D, as recited below.

"The diodes therefore provide for preventing the control gate region of each cell from reaching a potential which may damage the tunnel oxide. Before such a potential is reached, in fact, the diodes become conductive and discharge any excess charges,

which may result in an increase in potential in relation to the substrate, thus ensuring a safe maximum potential of the control gate regions. By virtue of the diodes being formed prior to patterning the polysilicon layer forming the control gate regions together with the silicide layer, the diodes are effective prior to performing the process that may result in an increase in potential of the polysilicon layer."

Accordingly, the two paragraphs include nothing related to the resistance of the composite line 23/24 between the word line 7 and the doped region 29.

Moreover, it is quite reasonable to suppose that ***the composite line 23/24 between the word line 7 and the doped region 29 has the same resistance as the word line 7***, since the word line 7 and the composite line 23/24 have the same material and thickness and their widths are never mentioned in the specification. In fact, the composite line 23/24 between the word line 7 and the doped region 29 ***does not need a high resistance*** since it is not blown after the fabricating process as in this invention. The leakage from the composite line 23/24 is controlled by the diode D in Cappelletti, while in this invention ***the poly-Si protection line having a high resistance is blown after the fabricating process to completely eliminate the leakage.***

In addition, it is not reasonable to take the poly-Si layer 23 from the composite line 23/24 between the word line 7 and the diode D as a poly-Si protection line, since the poly-Si layer 23 does not conduct electricity alone but surely together with the silicide layer 24 thereon, while the silicide layer 24 even shares more electric current for having a much lower resistance. In other words, it is meaningless to consider the electrical properties of the poly-Si layer 23 only without taking those of the silicide layer 24 into account.

For at least the reasons mentioned above, Applicants respectfully submit that independent claim 1 patently defines over the prior art.

With respect to claim 2, the Office Action also considers that the contents in col. 4, line 53-col. 5, line 7 of Cappelletti indicate that the resistance of the poly-Si protection line is higher than that of the poly-Si line of the word line. However, as mentioned above, there is actually ***a polycide line, rather than a poly-Si line***, disposed between the word line 7 and the doped region 29, and the contents in col. 4, line 53-col. 5, line 7 of Cappelletti include nothing about the resistance of the polycide line.

For at least the reasons mentioned above and the same reasons provided for claim 1, Applicants respectfully submit that claim 2 dependent from claim 1 also patently defines over the prior art.

As for claims 3 and 5-8, Applicants respectfully submit that claims 3-8 dependent from claim 1 also patently define over the prior art for at least the same reasons provided for claim 1.

Discussion of Rejection of Claim 4 under 35 U.S.C. 103(a)

Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Cappelletti, in view of some existing knowledge in the art. Claim 4 is dependent from independent claim 1.

As mention above, Cappelletti fails to teach or suggest the above feature of claim 1, since the composite line 23 & 24 is a polycide (poly-Si+silicide) line but not a polysilicon line, the doped region 29 is a part of the diode D but not a grounded doped region, and col. 4, line 53-col.

5, line 7 and the other parts of Cappelletti's specification do not describe that the composite line 23 & 24 between the word line 7 and the doped region 29 has a higher resistance.

For at least the reasons mentioned above, Applicants respectfully submit that claim 4 dependent from claim 1 also patently defines over the prior art.

CONCLUSION

For at least the foregoing reasons, it is believed that pending claims 1-8 are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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